

100V 2.2A N-Channel Enhancement Mode Power MOSFET

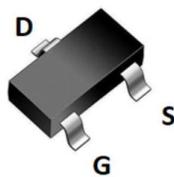
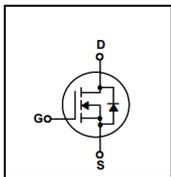
General Description

This Power MOSFET has been developed using advanced trench process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

FEATURES

- $R_{DS(ON)} \leq 280m\Omega$ @ $V_{GS}=10V, I_D=2A$
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

SYMBOL



SOT-23 top view

ASSEMBLY MESSAGE

| Product Name | Marking | Package | Packaging |
|--------------|---------|---------|-----------|
| BXT2800N10M | 0102 | SOT-23 | Reel |

ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$ unless otherwise noted)

| Parameter | | Symbol | Rating | Unit |
|------------------------------|--|-----------|------------|------------------|
| | | | SOT-23 | |
| Drain-Source Voltage | | V_{DSS} | 100 | V |
| Drain Current | Continuous ($T_C = 25^\circ\text{C}$) | I_D | 2.2 | A |
| | Continuous ($T_C = 100^\circ\text{C}$) | | 1.4 | A |
| Drain Current | Pulsed (Note1) | I_{DM} | 8.8 | A |
| Gate-Source Voltage | | V_{GSS} | ± 20 | V |
| Power Dissipation | $T_C = 25^\circ\text{C}$ | P_D | 2.8 | W |
| Maximum Junction Temperature | | T_J | 150 | $^\circ\text{C}$ |
| Storage Temperature Range | | T_{STG} | -55 to 150 | $^\circ\text{C}$ |

Note: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

THERMAL CHARACTERISTICS

| Parameter | Symbol | Max. | Unit |
|--|------------------|--------|--------|
| | | SOT-23 | |
| Thermal Resistance, Junction-to- Ambient | R _{θJA} | 44 | °C / W |

ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise Noted)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|--|---------------------|-------------------------------------|------|------|------|------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | VGS=0V, ID=250μA | 100 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | VDS=100V, VGS=0V | | | 1 | μA |
| Gate-Body Leakage Current, Forward | I _{GSS} | VGS=20V | | | 100 | nA |
| Gate-Body Leakage Current, Reverse | | VGS=-20V | | | -100 | nA |
| ON CHARACTERISTICS | | | | | | |
| Gate Threshold Voltage | VGS(TH) | VDS=VGS, ID=250μA | 1.0 | 2.1 | 3.0 | V |
| Drain-Source On-State Resistance | R _{DS(ON)} | VGS=10V, ID=2A | | 243 | 280 | mΩ |
| | | VGS=4.5V, ID=1A | | 259 | 310 | mΩ |
| DYNAMIC PARAMETERS | | | | | | |
| Input Capacitance | C _{ISS} | VDS=50V, VGS=0V, f=1.0MHz | | 360 | | pF |
| Output Capacitance | C _{OSS} | | | 24 | | pF |
| Reverse Transfer Capacitance | C _{RSS} | | | 13 | | pF |
| SWITCHING PARAMETERS | | | | | | |
| Turn-ON Delay Time | t _{D(ON)} | VDD=50V, ID=1A, VGS = 10V, RG=3Ω | | 14 | | ns |
| Turn-ON Rise Time | t _R | | | 54 | | ns |
| Turn-OFF Delay Time | t _{D(OFF)} | | | 18 | | ns |
| Turn-OFF Fall-Time | t _F | | | 11 | | ns |
| Total Gate Charge(Note2) | Q _G | VDS =50V, VGS =10V, ID =2A | | 12 | | nC |
| Gate Source Charge | Q _{GS} | | | 1.8 | | nC |
| Gate Drain Charge | Q _{GD} | | | 2.9 | | nC |
| SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS | | | | | | |
| Drain-Source Diode Forward Voltage | V _{SD} | IS=2.2A, VGS=0V | | | 1.2 | V |
| Diode Continuous Forward Current | I _S | | | | 2.2 | A |

Note: 2. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

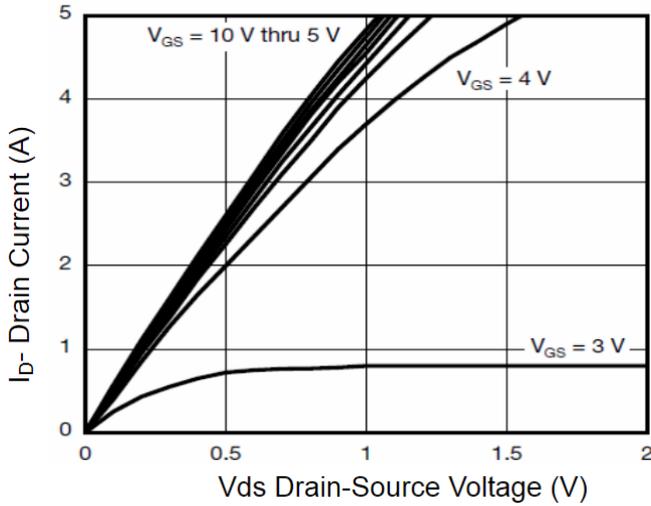


Fig 1: On-Region Characteristics

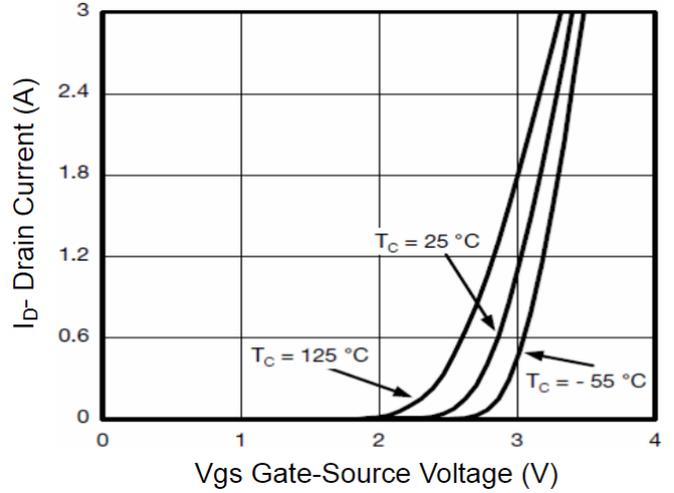


Figure 2: Transfer Characteristics

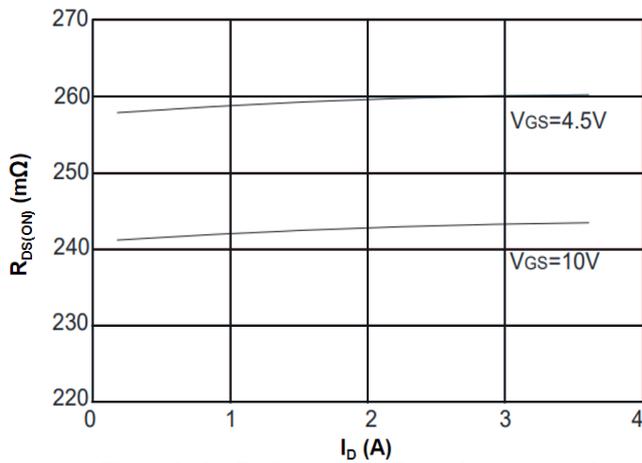


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

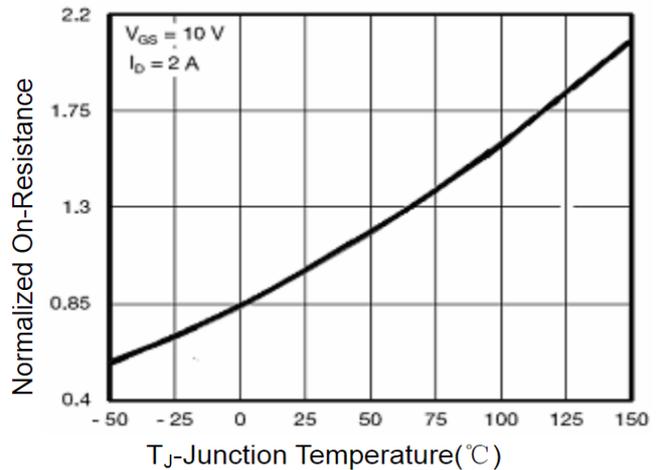


Figure 4: On-Resistance vs. Junction Temperature

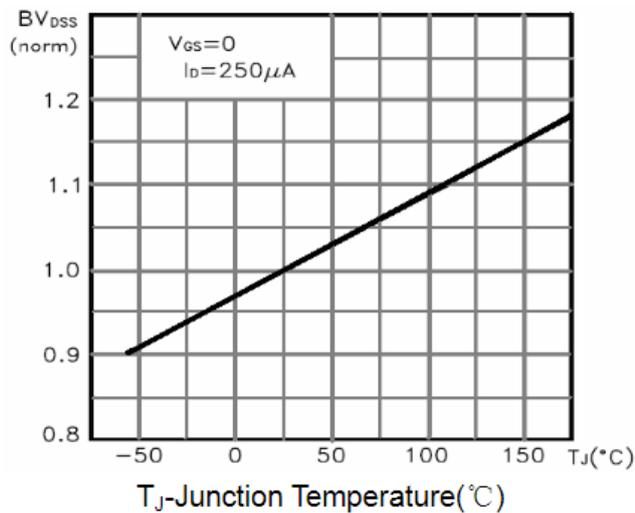


Figure 5 BV_{DSS} vs Junction Temperature

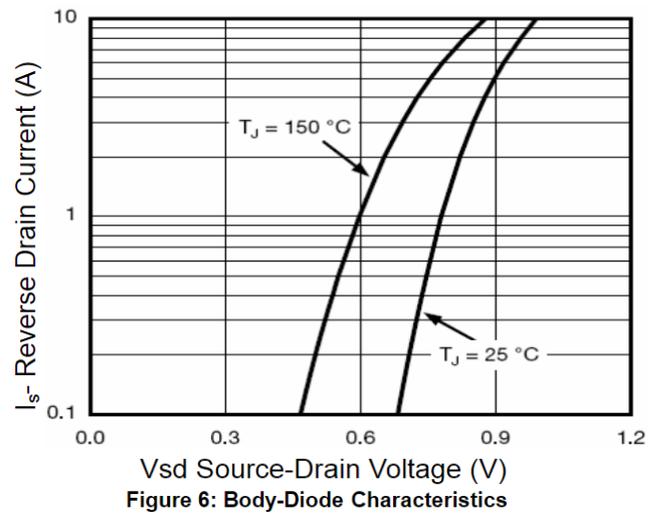


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS(Cont.)

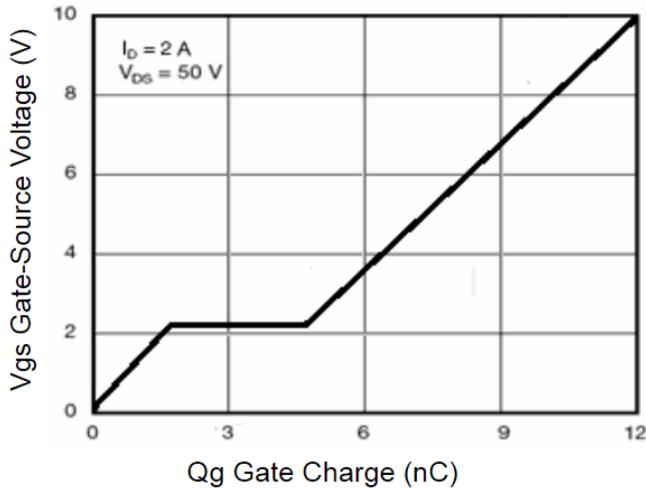


Figure 7: Gate-Charge Characteristics

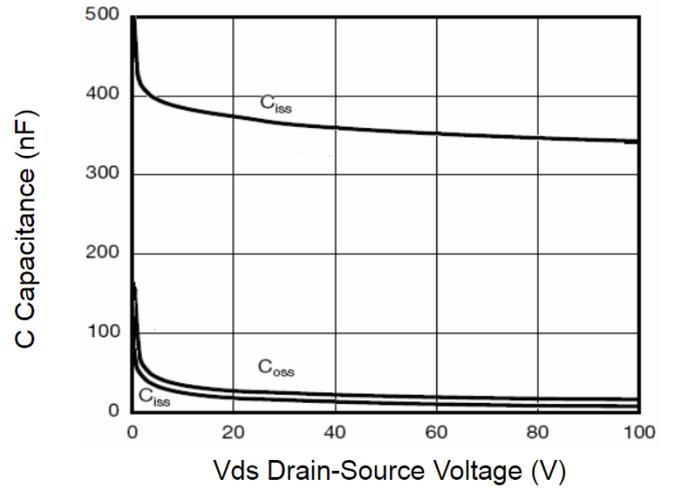


Figure 8: Capacitance Characteristics

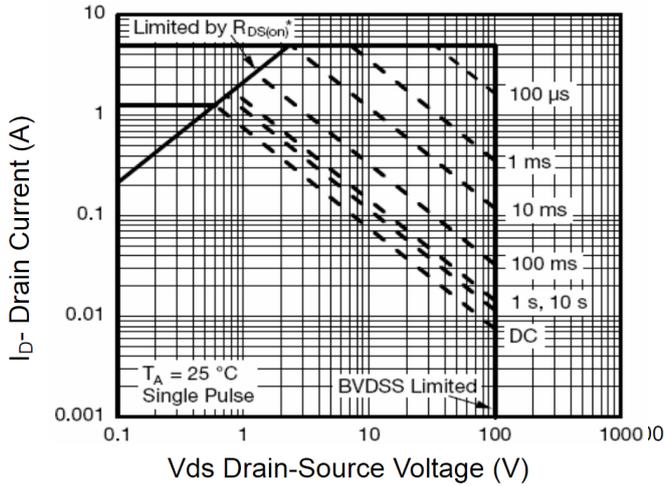
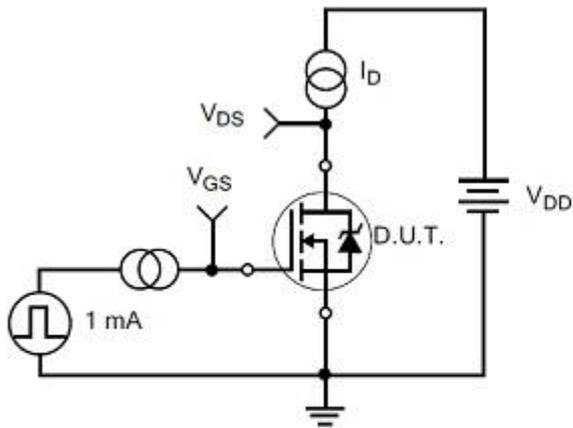
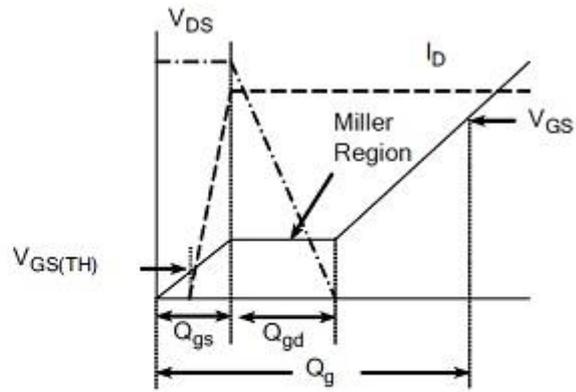


Figure 9: Maximum Forward Biased Safe Operating Area

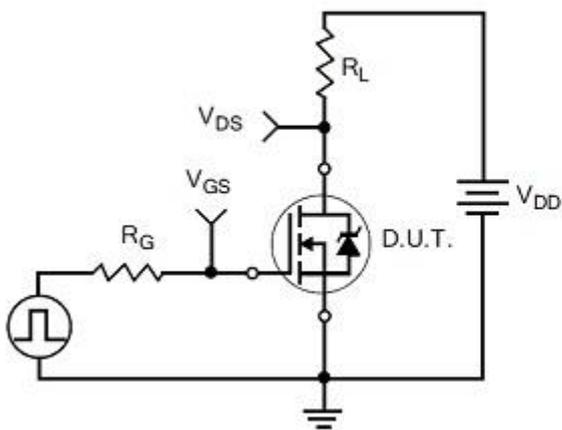
TEST CIRCUITS AND WAVEFORMS



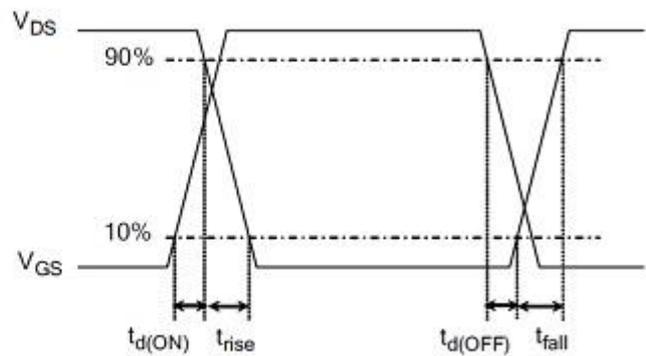
Gate Charge Test Circuit



Gate Charge Waveform

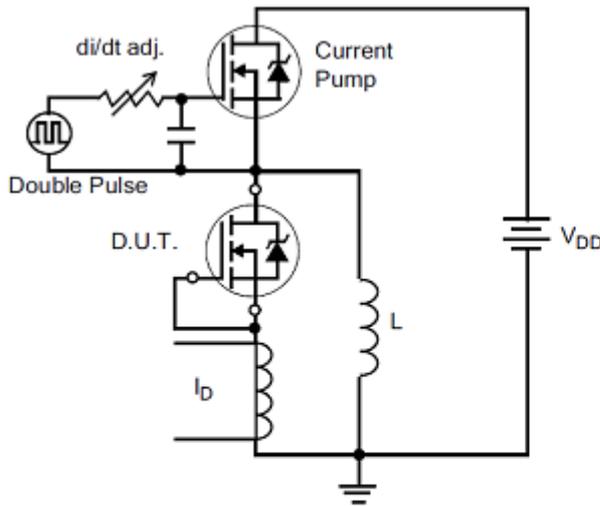


Resistive Switching Test Circuit

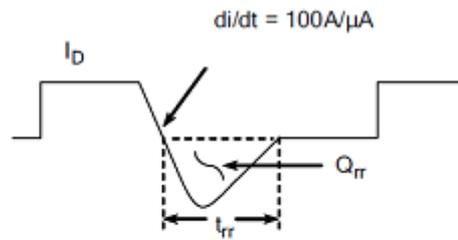


Resistive Switching Waveforms

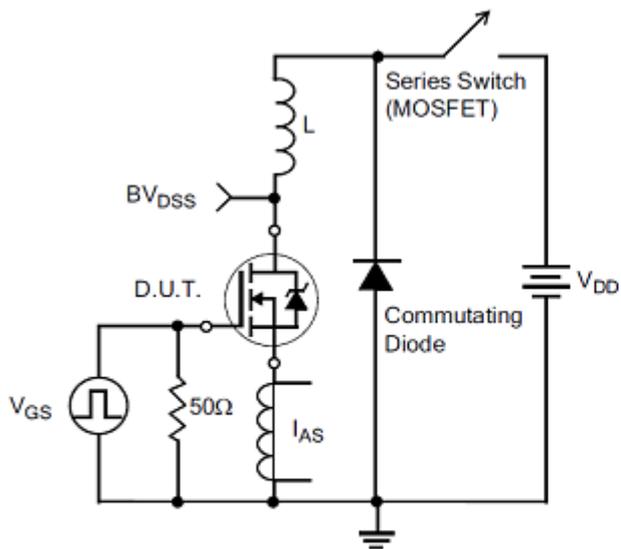
TEST CIRCUITS AND WAVEFORMS(Cont.)



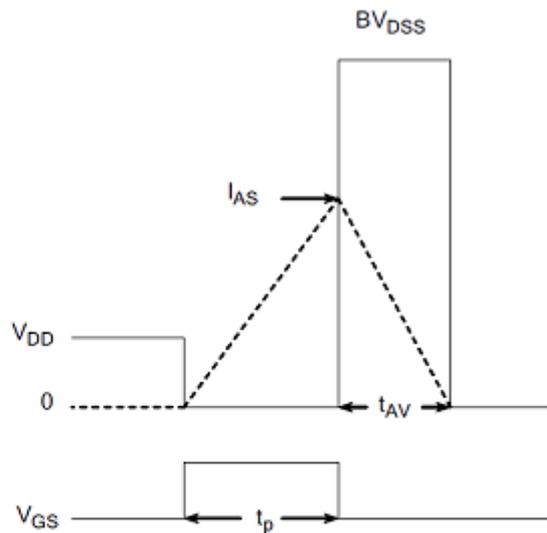
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



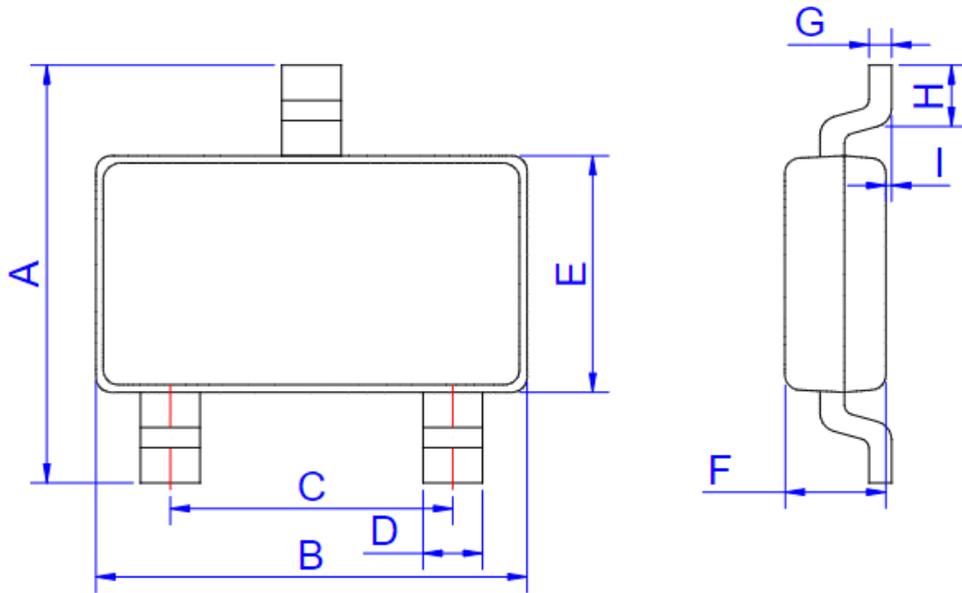
Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Unclamped Inductive Switching Waveforms

SOT-23 Package



SOT-23

| Ref. | Dimensions | | | |
|------|-------------|-------|--------|-------|
| | Millimeters | | Inches | |
| | Min. | Max. | Min. | Max. |
| A | 2.250 | 2.550 | 0.089 | 0.100 |
| B | 2.800 | 3.000 | 0.110 | 0.118 |
| C | 1.800 | 2.000 | 0.071 | 0.079 |
| D | 0.300 | 0.500 | 0.012 | 0.020 |
| E | 1.200 | 1.400 | 0.047 | 0.055 |
| F | 0.900 | 1.150 | 0.035 | 0.045 |
| G | | 0.200 | | 0.008 |
| H | 0.200 | | 0.008 | |
| I | 0.000 | 0.150 | 0.000 | 0.006 |

Revision history

Document revision history

| Date | Revision | Changes |
|-------------|----------|---------------|
| 28-Oct-2020 | 1.0 | First release |
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